AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) An integrated circuit comprising:

a transmitter to transmit a first signal to another integrated circuit, wherein the transmitter has a transmitter buffer ~~having~~ including a transmitter buffer output and a transmitter buffer input;

a receiver to receive a second signal from the other integrated circuit, wherein the receiver has a receiver buffer ~~having~~ including a receiver buffer output and a receiver buffer input, and wherein the receiver buffer input is coupled to the transmitter buffer output; ~~and~~

a differential buffer coupled between the transmitter buffer input and the receiver buffer output, wherein the differential buffer is configured to accept a third signal from the transmitter buffer input ~~of the transmit buffer~~ and to adjust the third signal in phase and amplitude to cancel the first signal at the ~~output of the~~ receiver buffer output; ~~.~~ and

a training circuit to set phase and amplitude characteristics of the differential buffer by determining which phase and amplitude characteristics minimize peak-to-peak noise at the receiver buffer output upon introduction of a training signal to the transmitter.

2. (Currently Amended) The integrated circuit ~~according to~~of claim 1, wherein the third signal is further adjusted in rise time.

3. (Currently Amended) The integrated circuit ~~according to~~of claim 1, wherein the training circuit comprises a ~~gain and phase characteristics of the differential buffer are varied by means of a~~ finite state machine ~~using a training pattern following either power up or a request~~.

4. (Currently Amended) The integrated circuit ~~according to~~of claim 3, wherein the differential buffer ~~is implemented as~~comprises a chain of buffer stages.

5. (Currently Amended) The integrated circuit ~~according to~~of claim [[4]]3, wherein the training circuit further ~~comprising~~ comprises one or more analog-to-digital converters coupled between the finite state machine and the differential buffer~~,~~ and a peak detector coupled between the finite state machine and the receiver buffer output ~~of the receiver~~, and wherein the finite state

machine is configured to vary the gain and phase characteristics of the differential buffer by reading ~~-~~a parameter from the peak detector, via the analog-to-digital converters, and is configured to set a value on the ~~digital-to-analogue~~ analog-to-digital converters to control one or more variable current sources ~~in~~ of the ~~chain of~~differential buffer ~~stages~~ based, at least in part, on the read parameter.

6. (Currently Amended) The integrated circuit ~~according to~~of claim 1, wherein the differential buffer has a variable current source to allow control of the amplitude or phase characteristics of the differential buffer.

7. (Currently Amended) The integrated circuit ~~according to~~of claim 1, ~~further comprising~~ awherein the ~~finite state machine~~training circuit is configured to set a programmable or variable load of the differential buffer to ~~control~~ set ~~of~~ the amplitude or phase characteristics of the differential buffer.

8. (Currently Amended) The integrated circuit ~~according to~~of claim 1, wherein the differential buffer includes a coarse delay circuit, a fine delay circuit, an amplitude control circuit, and a rise-time control circuit, and wherein the ~~integrated circuit further comprises a finite state machine~~training circuit is configured to control the coarse delay circuit, the fine delay circuit, the amplitude control circuit, and the rise-time control circuit to ~~vary~~ set the phase and amplitude characteristics of the differential buffer to adjust the third signal in phase and amplitude and to cancel ~~the~~ a ~~first~~ signal echo component of the second signal at the receiver buffer output ~~of the receiver buffer~~.

9. (Currently Amended) The integrated circuit ~~according to~~of claim ~~8~~1, wherein the ~~finite state machine~~training circuit is configured to vary the phase and amplitude characteristics of the differential buffer as part of a calibration procedure initiated following ~~power~~ power-up or after being initiated on request.

10. (Canceled)

11. (Currently Amended) The integrated circuit ~~according to~~of claim 8, wherein the coarse delay circuit comprises a digital delay line, a pair of multiplexers, and logic to control the multiplexers.

12. (Currently Amended) The integrated circuit ~~according to~~of claim 11, wherein the digital delay line comprises a cascade of buffers.

13. (Currently Amended) The integrated circuit ~~according to~~of claim 11, further comprising a pair of multiplexers configured to select signals from the digital delay line.

14. (Currently Amended) The integrated circuit ~~according to~~of claim 9, wherein the ~~finite state machine~~ training circuit is configured to generate control signals to be used to select signals from the digital delay line in the coarse delay circuit to vary the delay of the third signal through the differential buffer.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) The integrated circuit ~~according to~~of claim 1, further comprising ~~a finite state machine and an~~ analog-to-digital converter ~~(ADC)~~ coupled to the training circuit, wherein the analog-to-digital converter ~~to~~ provides a control voltage to the differential buffer to vary the amplitude of the third signal.

18. (Currently Amended) The integrated circuit ~~according to~~of claim 8, wherein the amplitude control circuit comprises a buffer with a variable load.

19. (Currently Amended) The integrated circuit ~~according to~~of claim 18, wherein the ~~finite state machine~~training circuit is configured to control a gate voltage of an NMOS transistor to vary the variable load.

20. (Currently Amended) The integrated circuit ~~according to~~of claim 8, wherein the rise-time control circuit comprises switches, capacitors, and control logic.

21. (Currently Amended) The integrated circuit ~~according to~~of claim 9, wherein the ~~finite state machine~~training circuit is configured to generate control signals ~~to~~ for the rise-time control circuit to vary the rise-time of the third signal.

22. (Currently Amended) The integrated circuit ~~according to~~of claim 5, wherein the peak detector comprises an amplitude cancellation sensor, a phase cancellation sensor, and an ~~analogue~~ analog multiplexer.

23. (Currently Amended) The integrated circuit ~~according to~~of claim 22, wherein the finite state machine is configured to adjust another amplitude and/or another phase characteristic of the other integrated circuit during a calibration phase.

24. (Currently Amended) The integrated circuit ~~according to~~of claim 22, wherein the amplitude cancellation sensor comprises an integrator and a ~~sample~~ sample-~~and~~ and-hold device.

25. (Currently Amended) The integrated circuit ~~according to~~of claim 22, wherein the phase cancellation sensor is configured to cycle through a reset phase, an integration phase, and a transfer phase during a calibration phase.

26. (Currently Amended) The integrated circuit ~~according to~~of claim 25, wherein the finite state machine is configured to control the timing of the phases.

27. (Currently Amended) The integrated circuit ~~according to~~of claim 22, wherein the finite state machine is further configured to inject patterns into the transmitter and to measure a resulting offset in the amplitude cancellation sensor.

28. (Currently Amended) The integrated circuit ~~according to~~of claim 22, wherein the phase cancellation sensor comprises a full-wave rectifier plus integrator and a ~~sample~~ sample-~~and~~ and-hold circuit.

29. (Currently Amended) The integrated circuit ~~according to~~of claim 24, wherein the integrator is configured to cycle through a reset phase, an integration phase, and a transfer phase.

30. (Currently Amended) The integrated circuit ~~according to~~of claim 28, wherein the finite state machine is configured to control the timing of the phases for the phase cancellation sensor.

31. (Canceled).

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Currently Amended) ~~A~~ The method ~~comprising~~of claim 39, further comprising:

transmitting a first signal from ~~an~~ the output buffer of ~~a~~ the transmitter ~~arranged on an integrated circuit,~~ to another circuit, wherein the first signal ~~being~~ is also coupled ~~also~~ into an input buffer of ~~a~~ the receiver ~~arranged on the integrated circuit~~;

receiving a second signal from the other ~~integrated~~ circuit;

transmitting a third signal from ~~the an~~the input buffer of the transmitter ~~buffer~~ through ~~a~~ the differential buffer;

adjusting, ~~by~~ via the differential buffer, the third signal in phase and amplitude; and

coupling the adjusted third signal ~~onto the output of the~~into ~~an~~ the output buffer of the receiver to cancel a ~~first~~ signal echo component of the second signal.

36. (Currently Amended) The~~A~~ method ~~according to~~of claim 35, wherein a third phase of the third signal is opposite to a first phase of the first signal.

37. (Currently Amended) The~~A~~ method ~~according to~~of claim 35, wherein a third rise time of the third signal is adjusted to match a first rise time of the first signal.

38. (Currently Amended) The~~A~~ method ~~according to~~of claim 35, wherein a gain property of the differential buffer is varied, at least in part, by using a training pattern.

39. (Currently Amended) A method ~~according to claim 35 wherein adjusting the phase and/or amplitude of the third signal comprises~~ comprising:

applying a training pattern to ~~the~~ an input of ~~the~~ a transmitter~~,~~;

varying a digital-to-analog code being applied to a digital-to-analog converter ~~(DAC)~~ to adjust operating parameters of ~~the~~ a differential buffer~~,~~;

measuring resulting noise conditions at an output buffer of a receiver coupled to an input buffer of the transmitter, wherein the noise conditions correspond~~ing~~ to each applied digital-to-analog code~~,~~;

determining a ~~digital to analog~~digital-to-analog code that corresponds to a minimum noise condition~~,~~; and

applying the determined code to the ~~Digital to Analog~~digital-to-analog c~~C~~onverter to calibrate the differential buffer.

40. (Canceled)